19-3649; Rev 5; 12/09

Overvoltage Protection Controllers with Low Standby Current

General Description

The MAX4843–MAX4846 overvoltage protection controllers protect low-voltage systems against high-voltage faults of up to 28V. When the input voltage exceeds the overvoltage threshold, these devices turn off a low-cost, external n-channel FET(s) to prevent damage to the protected components. An internal charge pump eliminates the need for external capacitors and drives the FET gate for a simple, robust solution.

The overvoltage trip level is set to 7.4V (MAX4843), 6.35V (MAX4844), 5.8V (MAX4845), or 4.65V (MAX4846). When the input voltage drops below the undervoltage lockout (UVLO) threshold, the devices enter a low standby current mode (10µA). The MAX4843/MAX4844/MAX4845 have a UVLO threshold of 4.15V, the MAX4845C/MAX4845D have a UVLO threshold of 2.2V, and the MAX4846 has a UVLO threshold of 2.5V. In addition to the single FET configuration, the devices can be configured with back-to-back external FETs to prevent currents from being back-driven into the adapter.

An additional feature includes a ±15kV ESD-protected input when bypassed with a 1µF capacitor to ground. All devices are offered in small 6-pin µDFN (1.5mm x 1.0mm) and 6-pin ultra-thin LGA (MAX4845 and MAX4846 only) (1.5mm x 1.0mm) packages and are specified for operation over the -40°C to +85°C temperature range.

Applications

Cell Phones

Digital Still Cameras

PDAs and Palmtop Devices

MP3 Players

Features

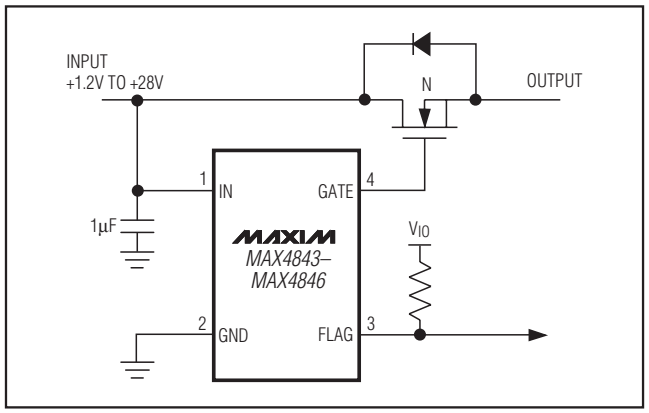
- **Overvoltage Protection Up to 28V**
- **Preset 7.4V, 6.35V, 5.8V, or 4.65V Overvoltage Trip Level**
- **Low (10µA) Undervoltage Lockout Standby Current**
- **Drives Low-Cost nMOSFET**
- **Internal 50ms Startup Delay**
- **Internal Charge Pump**
- **Overvoltage Fault FLAG Indicator**
- **6-Pin (1.5mm x 1.0mm) µDFN Package**

Ordering Information

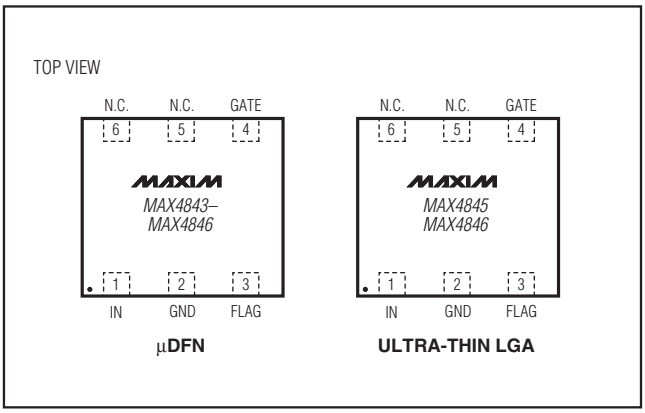
PART	PIN-PACKAGE	UVLO (V)	OVLO (V)	TOP MARK
MAX4843ELT	6 µDFN	4.15	7.40	BE
MAX4844ELT	6 µDFN	4.15	6.35	BF
MAX4845ELT	6 µDFN	4.15	5.80	BG
MAX4845EYT+T	6 UTLGA	4.15	5.80†	AC
MAX4845CEYT+T	6 UTLGA	2.20	5.80†	AP
MAX4845DEYT+T	6 UTLGA	2.20	5.80	AQ
MAX4846ELT	6 µDFN	2.50	4.65	BH
MAX4846EYT+T	6 UTLGA	2.50	4.65	AD

Note: *All devices are specified over the -40°C to +85°C temperature range.*
+Denotes a lead(Pb)-free/RoHS-compliant package.
T = Tape and reel.
†OVLO maximum is 6.0V for the MAX4845C and 5.9V for the MAX4845D.

Typical Operating Circuit



Pin Configurations



For pricing, delivery, and ordering information, please contact Maxim Direct at 1-888-629-4642, or visit Maxim's website at www.maxim-ic.com.

Overvoltage Protection Controllers with Low Standby Current

ABSOLUTE MAXIMUM RATINGS

IN to GND .....-0.3V to +30V
GATE to GND .....-0.3V to +12V
FLAG to GND .....-0.3V to +6V
Continuous Power Dissipation (T_A = +70°C)
6-Pin µDFN (derate 2.1mW/°C above +70°C) 167.7mW
6-Pin Ultra-Thin LGA (derate 2.1mW/°C above +70°C) 170.2mW

Operating Temperature Range .....-40°C to +85°C
Junction Temperature ..... +150°C
Storage Temperature Range .....-65°C to +150°C
Soldering Temperature (reflow)
6-Pin µDFN.....+240°C
6-Pin Ultra-Thin LGA.....+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{IN} = +5V for MAX4843/MAX4844/MAX4845, V_{IN} = +4V for MAX4846, C_{GATE} = 500pF, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Input Voltage Range	V_{IN}			1.2		28.0	V
Undervoltage Lockout Threshold	UVLO	V_{IN} falling	MAX4843/MAX4844/MAX4845	3.9	4.15	4.4	V
			MAX4845C/MAX4845D	1.8	2.2	2.5	
			MAX4846	2.3	2.5	2.7	
Undervoltage Lockout Hysteresis		MAX4843/MAX4844/MAX4845			41		mV
		MAX4846			25		
Overvoltage Trip Level	OVLO	V_{IN} rising	MAX4843	7.0	7.4	7.8	V
			MAX4844	6.0	6.35	6.7	
			MAX4845	5.5	5.8	6.1	
			MAX4845C	5.5	5.8	6.0	
			MAX4845D	5.5	5.8	5.9	
			MAX4846	4.35	4.65	4.95	
Overvoltage Lockout Hysteresis		MAX4843			75		mV
		MAX4844			65		
		MAX4845			55		
		MAX4846			50		
IN Supply Current	I_{IN}	MAX4843/MAX4844/MAX4845			70	120	µA
		MAX4846			60	110	
UVLO Supply Current	I_{UVLO}	V_{IN} = 3.8V	MAX4843/MAX4844/MAX4845		10	22	µA
		V_{IN} = 2.2V	MAX4846		8	18	
Gate Voltage	V_{GATE}	1µA load	MAX4843/MAX4844/MAX4845	9	9.83	10	V
			MAX4846	7.5	7.85	8.0	
GATE Pulldown Current	I_{PD}	V_{IN} > OVLO, V_{GATE} = 5.5V		10	27		mA
FLAG Output Low Voltage	V_{OL}	I_{SINK} = 1mA, FLAG deasserted				0.4	V
FLAG Leakage Current		V_{FLAG} = 5.5V, FLAG asserted				1	µA

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN} = +5V for MAX4843/MAX4844/MAX4845, V_{IN} = +4V for MAX4846, C_{GATE} = 500pF, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

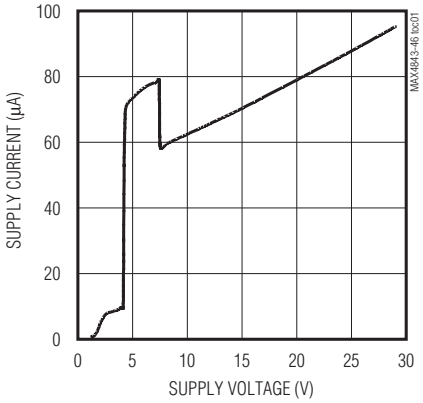
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
TIMING						
Startup Delay	t_{START}	V_{IN} = UVLO rising to V_{GATE} = 0.3V rising (Figure 1)	20	50	80	ms
FLAG Blanking Time	t_{BLANK}	V_{GATE} = 0.3V rising to V_{FLAG} = 0.3V falling (Figure 1)	20	50	80	ms
Gate Turn-On Time	t_{GON}	V_{GATE} = 0.3V to 8V (MAX4843/MAX4844/MAX4845), V_{GATE} = 0.3V to 7V (MAX4846) (Figure 1)		10		ms
Gate Turn-Off Time	t_{GOFF}	V_{IN} rising at 1V/µs from 5V to 8V (MAX4843/MAX4844/MAX4845) or from 4V to 7V (MAX4846) to V_{GATE} = 0.3V (Figure 2)		6	20	µs
FLAG Assertion Delay	t_{FLAG}	V_{IN} rising at 1V/µs from 5V to 8V (MAX4843/MAX4844/MAX4845) or from 4V to 7V (MAX4846), to V_{FLAG} = 2.4V, R_{FLAG} = 10k to 3V (Figure 2)		5.8		µs
Initial Overvoltage Fault Delay	t_{OVP}	V_{IN} rising at 1V/µs from 0V to 9V, time from V_{IN} = 5V to I_{GATE} = 80% of I_{PD} (Figure 3)		1.5		µs

Note 1: All devices are 100% tested at +25°C. Electrical limits across the full temperature range are guaranteed by design and correlation.

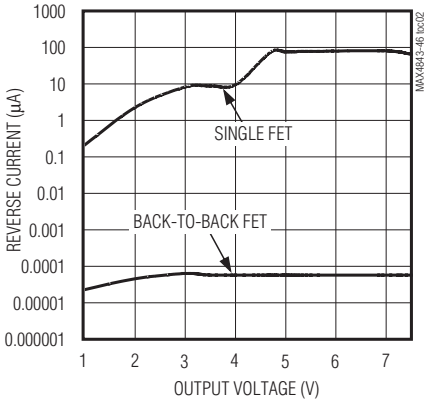
Typical Operating Characteristics

(V_{IN} = +5V for MAX4843/MAX4844/MAX4845, V_{IN} = +4V for MAX4846, T_A = +25°C, unless otherwise noted.)

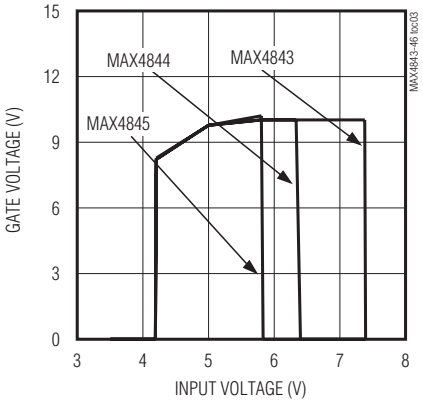
SUPPLY CURRENT vs. SUPPLY VOLTAGE (MAX4843)



REVERSE CURRENT vs. OUTPUT VOLTAGE (MAX4843)



GATE VOLTAGE vs. INPUT VOLTAGE (MAX4843/MAX4844/MAX4845)

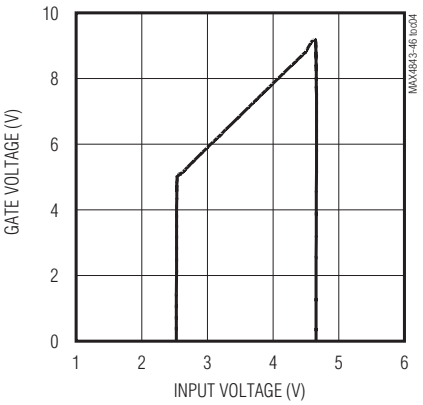


Overvoltage Protection Controllers with Low Standby Current

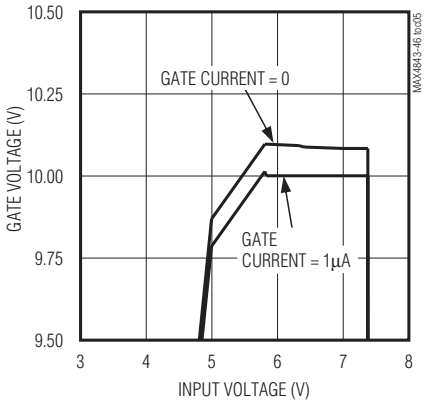
Typical Operating Characteristics (continued)

(V_{IN} = +5V for MAX4843/MAX4844/MAX4845, V_{IN} = +4V for MAX4846, T_A = +25°C, unless otherwise noted.)

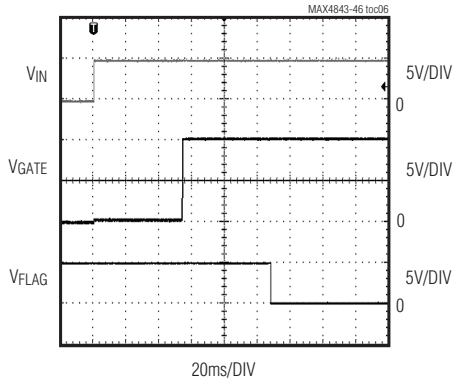
GATE VOLTAGE vs. INPUT VOLTAGE (MAX4846)



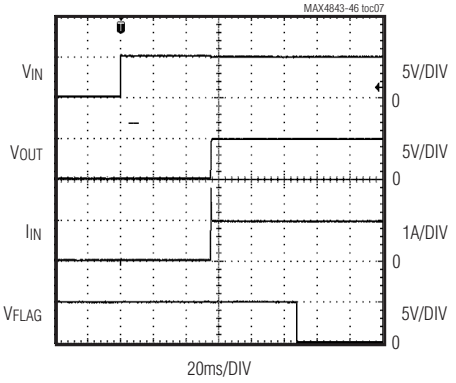
GATE VOLTAGE vs. INPUT VOLTAGE (MAX4843)



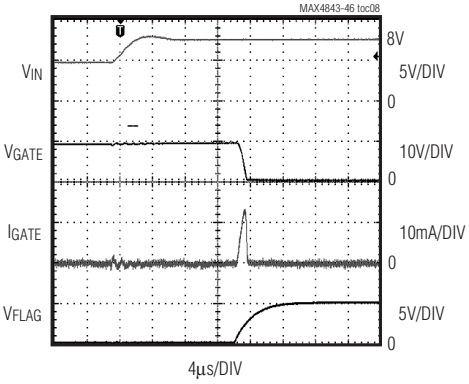
POWER-UP RESPONSE



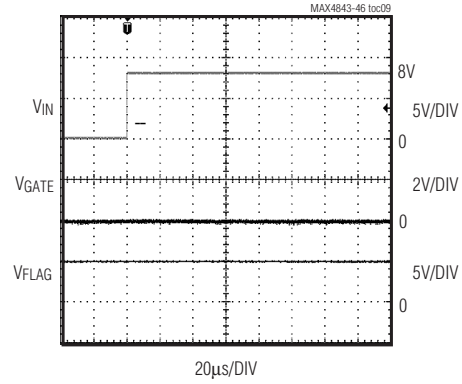
POWER-UP RESPONSE



OVERVOLTAGE RESPONSE



POWER-UP OVERVOLTAGE RESPONSE

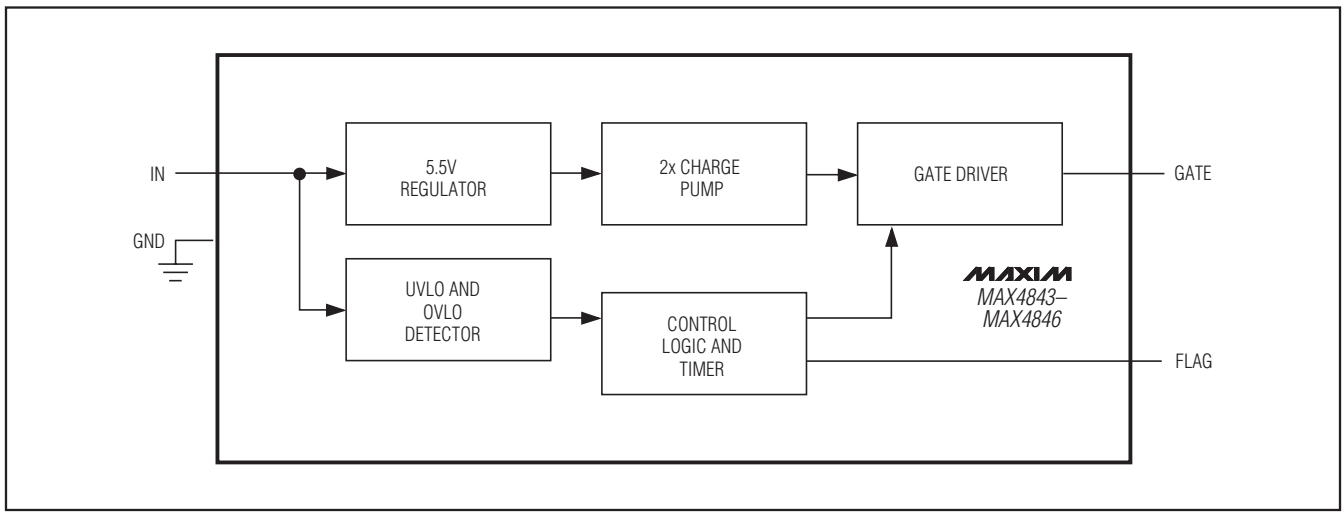


Pin Description

PIN		NAME	FUNCTION
µDFN	ULTRA-THIN LGA		
1	1	IN	Voltage Input. IN is both the power-supply input and the overvoltage sense input. Bypass IN to GND with a 1µF capacitor or larger.
2	2	GND	Ground
3	3	FLAG	Fault Indication Output. FLAG is asserted high during undervoltage lockout and overvoltage lockout conditions. FLAG is deasserted during normal operation. FLAG is an open-drain output.
4	4	GATE	Gate-Drive Output. GATE is the output of an on-chip charge pump. When $V_{UVLO} < V_{IN} < V_{OVLO}$, GATE is driven high to turn on the external n-channel MOSFET(s).
5, 6	5, 6	N.C.	No Connection. Not internally connected. Do not connect.

Overvoltage Protection Controllers with Low Standby Current

Functional Diagram



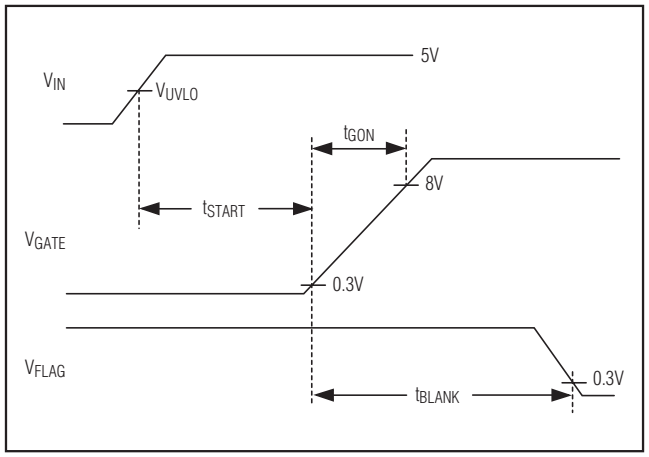


Figure 1. Startup Timing Diagram

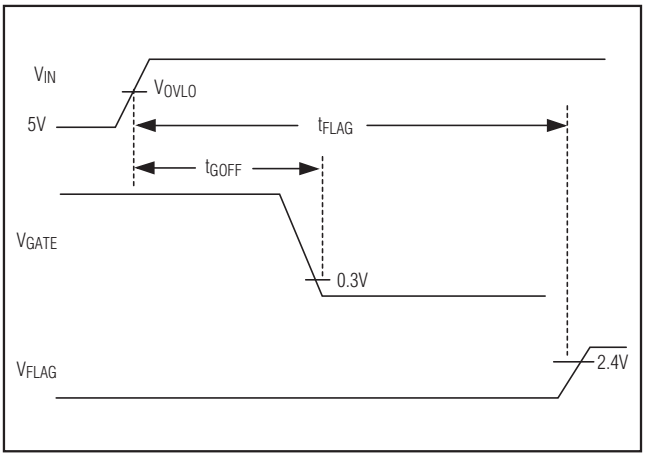


Figure 2. Shutdown Timing Diagram

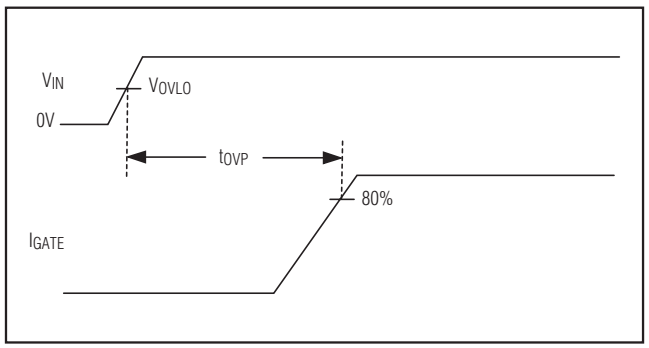


Figure 3. Power-Up Overvoltage Timing Diagram

Overvoltage Protection Controllers with Low Standby Current

Detailed Description

The MAX4843–MAX4846 provide up to 28V overvoltage protection for low-voltage systems. When the input voltage exceeds the overvoltage trip level, the MAX4843–MAX4846 turn off a low-cost external n-channel FET(s) to prevent damage to the protected components. An internal charge pump (see the *Functional Diagram*) drives the FET gate for a simple, robust solution. On power-up, the device waits for 50ms before driving GATE high. The open-drain FLAG output is kept at high impedance for an additional 50ms after GATE goes high before deasserting. The FLAG output asserts high immediately to an overvoltage fault.

Undervoltage Lockout (UVLO)

The MAX4843/MAX4844/MAX4845 have a fixed 4.15V typical UVLO level, the MAX4845C/MAX4845D have a 2.2V typical UVLO, and the MAX4846 has a 2.5V typical UVLO. When V_{IN} is less than the UVLO, the GATE driver is held low and FLAG is asserted.

Overvoltage Lockout (OVLO)

The MAX4843 has a 7.4V typical OVLO; the MAX4844 has a 6.35V typical OVLO; and the MAX4845 has a 5.8V typical OVLO. The MAX4846 has a 4.65V typical overvoltage threshold. When V_{IN} is greater than OVLO, the GATE driver is held low and FLAG is asserted.

FLAG Output

The open-drain FLAG output is used to signal to the host system that there is a fault with the input voltage. FLAG asserts immediately to an overvoltage fault. FLAG is held high for 50ms after GATE turns on before deasserting. Connect a pullup resistor from FLAG to the logic I/O voltage of the host system.

GATE Driver

An on-chip charge pump is used to drive GATE above IN, allowing the use of low-cost n-channel MOSFETs. The charge pump operates from the internal 5.5V regulator.

The actual GATE output voltage tracks approximately two times V_{IN} until V_{IN} exceeds 5.5V or the OVLO trip level is exceeded, whichever comes first. The MAX4843 has a 7.4V typical OVLO, therefore GATE remains relatively constant at about 10.5V for 5.5V < V_{IN} < 7.4V. The MAX4845 has a 5.8V typical OVLO, but this can be as low as 5.5V. The GATE output voltage as a function of input voltage is shown in the *Typical Operating Characteristics*.

Device Operation

The MAX4843–MAX4846 have an on-board state machine to control device operation. A flowchart is shown in Figure 4. On initial power-up, if V_{IN} < UVLO or if V_{IN} > OVLO, GATE is held at 0V, and FLAG is high.

If UVLO < V_{IN} < OVLO, the device enters startup after a 50ms internal delay. The internal charge pump is enabled, and GATE begins to be driven above V_{IN} by the internal charge pump. FLAG is held high during startup until the FLAG blanking period expires, typically 50ms after the GATE starts going high. At this point the device is in its on state.

At any time if V_{IN} drops below UVLO or V_{IN} is greater than OVLO, FLAG is driven high and GATE is driven to ground.

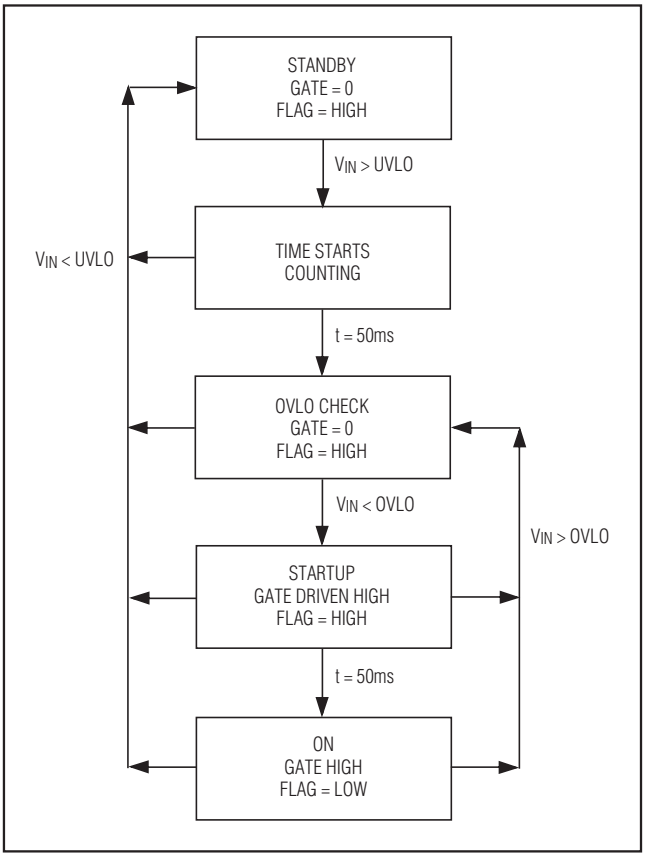


Figure 4. State Diagram

Applications Information

MOSFET Configuration

The MAX4843–MAX4846 can be used with either a single MOSFET configuration as shown in the *Typical Operating Circuit*, or can be configured with a back-to-back MOSFET as shown in Figure 5. The back-to-back configuration has almost zero reverse current when the input supply is below the output.

If reverse current leakage is not a concern, a single MOSFET can be used. This approach has half the loss of the back-to-back configuration when used with similar MOSFET types and is a lower cost solution. Note that if the input is actually pulled low, the output is also pulled low due to the parasitic body diode in the MOSFET. If this is a concern, the back-to-back configuration should be used.

In a typical application of the MAX4846, an external adapter with built-in battery charger is connected to IN and a battery is connected to the source of the external FET. When the adapter is unplugged, IN is directly connected to the battery through the external FET. Since the battery voltage is typically greater than 3V, the GATE voltage stays high and the device remains powered by the battery.

MOSFET Selection

The MAX4843–MAX4846 are designed for use with either a single n-channel MOSFET or dual back-to-back n-channel MOSFETs. In most situations, MOSFETs with R_{ON} specified for a V_{GS} of 4.5V work well. If the input supply is near the UVLO maximum of 3.5V, consider using a MOSFET specified for a lower V_{GS} voltage. Also the V_{DS} should be 30V for the MOSFET to withstand the full 28V IN range of the MAX4843–MAX4846. Table 1 shows a selection of MOSFETs appropriate for use with the MAX4843–MAX4846.

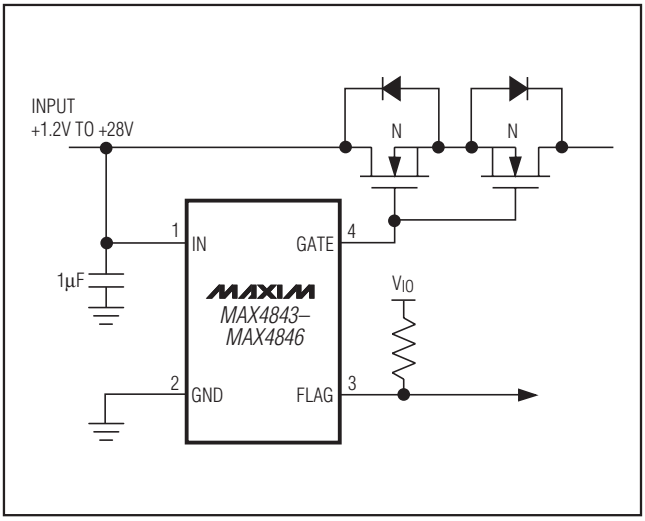


Figure 5. Back-to-Back External MOSFET Configuration

IN Bypass Considerations

For most applications, bypass IN to GND with a 1µF ceramic capacitor. If the power source has significant inductance due to long lead length, take care to prevent overshoots due to the LC tank circuit and provide protection if necessary to prevent exceeding the 30V absolute maximum rating on IN.

The MAX4843–MAX4846 provide protection against voltage faults up to 28V, but this does not include negative voltages. If negative voltages are a concern, connect a Schottky diode from IN to GND to clamp negative input voltages.

ESD Test Conditions

ESD performance depends on a number of conditions. The MAX4843–MAX4846 are protected from ±15kV typical ESD on IN when IN is bypassed to ground with a 1µF ceramic capacitor.

Table 1. MOSFET Suggestions

PART	CONFIGURATION/ PACKAGE	V_{DS} MAX (V)	R_{ON} at 4.5V (mΩ)	MANUFACTURER
Si5902DC	Dual/1206-8	30	143	Vishay Siliconix www.vishay.com
Si1426DH	Single/SSOT-6	30	115	
FDC6561AN	Dual/SSOT-6	30	145	Fairchild Semiconductor www.fairchildsemi.com
FDC6305N	Dual/SSOT-6	20	80	

Overvoltage Protection Controllers with Low Standby Current

Human Body Model

Figure 6 shows the Human Body Model and Figure 7 shows the current waveform it generates when discharged into a low impedance. This model consists of a 100pF capacitor charged to the ESD voltage of interest, which is then discharged into the device through a 1.5kΩ resistor.

IEC 1000-4-2

Since January 1996, all equipment manufactured and/or sold in the European Union has been required to meet the stringent IEC 1000-4-2 specification. The IEC 1000-4-2 standard covers ESD testing and performance of finished equipment; it does not specifically refer to integrated circuits. The MAX4843–MAX4846 help users design equipment that meets Level 3 of IEC 1000-4-2, without additional ESD-protection components.

The main difference between tests done using the Human Body Model and IEC 1000-4-2 is higher peak current in IEC 1000-4-2. Because series resistance is lower in the IEC 1000-4-2 ESD test model (Figure 8), the ESD withstand voltage measured to this standard is generally lower than that measured using the Human Body Model. Figure 9 shows the current waveform for the ±8kV IEC 1000-4-2 Level 4 ESD Contact Discharge test. The Air-Gap test involves approaching the device with a charger probe. The Contact Discharge method connects the probe to the device before the probe is energized.

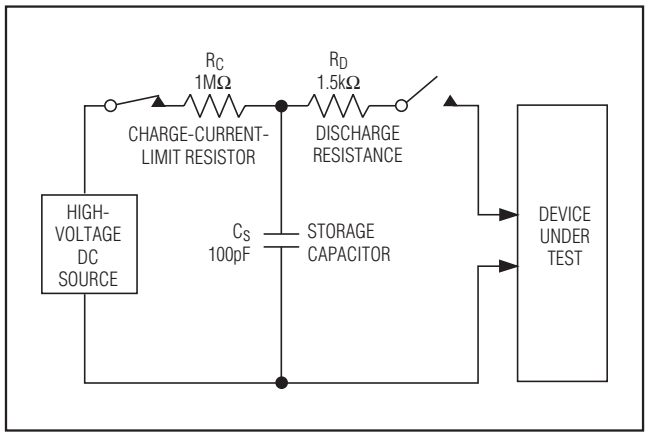


Figure 6. Human Body ESD Test Model

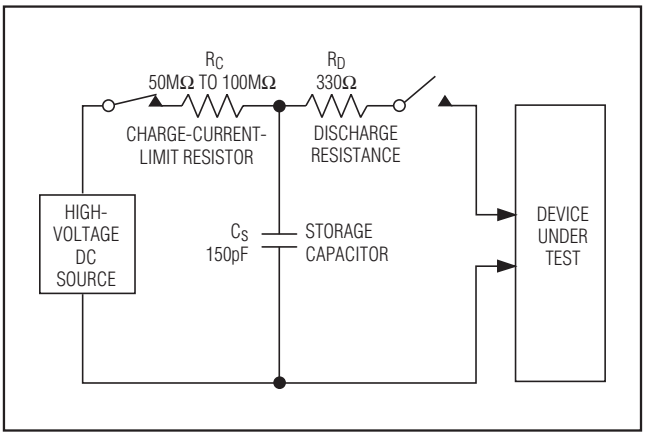


Figure 8. IEC 1000-4-2 ESD Test Model

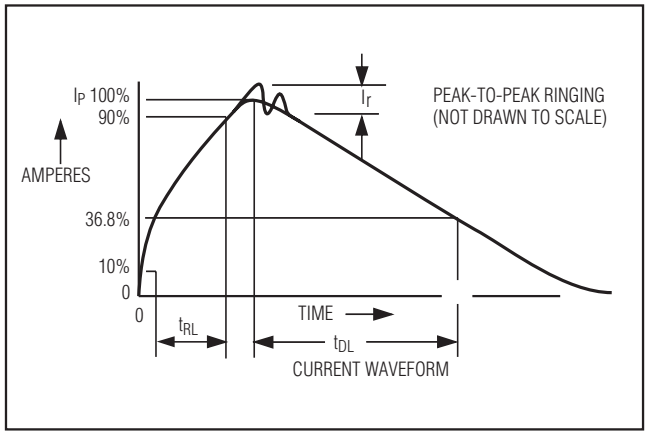


Figure 7. Human Body Model Current Waveform

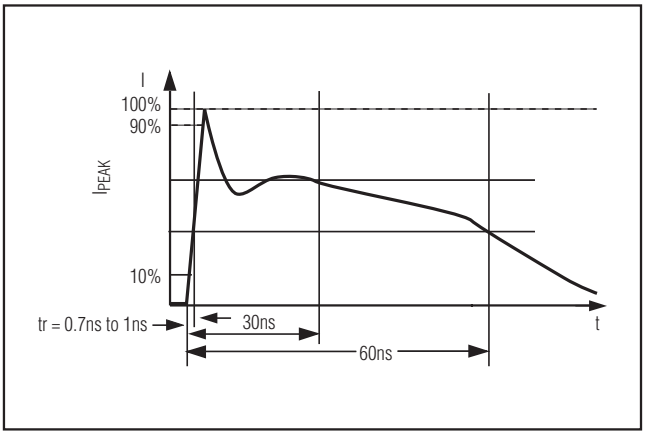


Figure 9. IEC 1000-4-2 ESD Generator Current Waveform

Chip Information

PROCESS: BiCMOS

Package Information

For the latest package outline information and land patterns, go to **www.maxim-ic.com/packages**.

PACKAGE TYPE	PACKAGE CODE	DOCUMENT NO.
6 µDFN	L611-1	**21-0147**
6 UTLGA	Y61A1-1	**21-0190**

Overvoltage Protection Switches with Low Standby Current

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	4/05	Initial release	—
3	2/08	Added packaging, removed SC70	1, 2, 4, 7, 9
4	8/09	Added MAX4845A and MAX4845C to *Ordering Information* and *Electrical Characteristics*.	1, 2
5	12/09	• Removed MAX4845A and added MAX4845D to *Ordering Information* and *Electrical Characteristics*. • Updated *Undervoltage Lockout (UVLO)* section under *Detailed Description* to include MAX4845D.	1, 2, 6

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